# STM32 – Digital IP Stage Activity

**Summary:**

Purpose of this activity is to link the design verification flow developed for the SPI2 interface embedded inside the STM32 H7 microcontrollers family with the silicon validation environment built in to assess the performances and functional behaviors of the SPI2 interface with the ultimate objective to reuse the verification patterns developed by design verification team to upgrade and improve the coverage effectiveness of bench validation environment.

**Requisites:**
- Master degree in "*Ingegneria Elettronica"* or "*Ingegneria Informatica"* (*Laurea specialistica*)

- Software programming language knowledge (c code), RTL (VHDL) Knowledge and ability to interpret the design implementation description,

- VLSI design knowledge

Nice to have:
- STM32 knowledge or experience

**Detail of the activity.**

The activity will be organized in different phases.

Phase 1

STM32 H7 series training
Definition of bench validation environment in line with silicon verification
Test patterns

Phase 2

validation execution phase using the bench environment at ST site

Phase 3

Analysis of results