

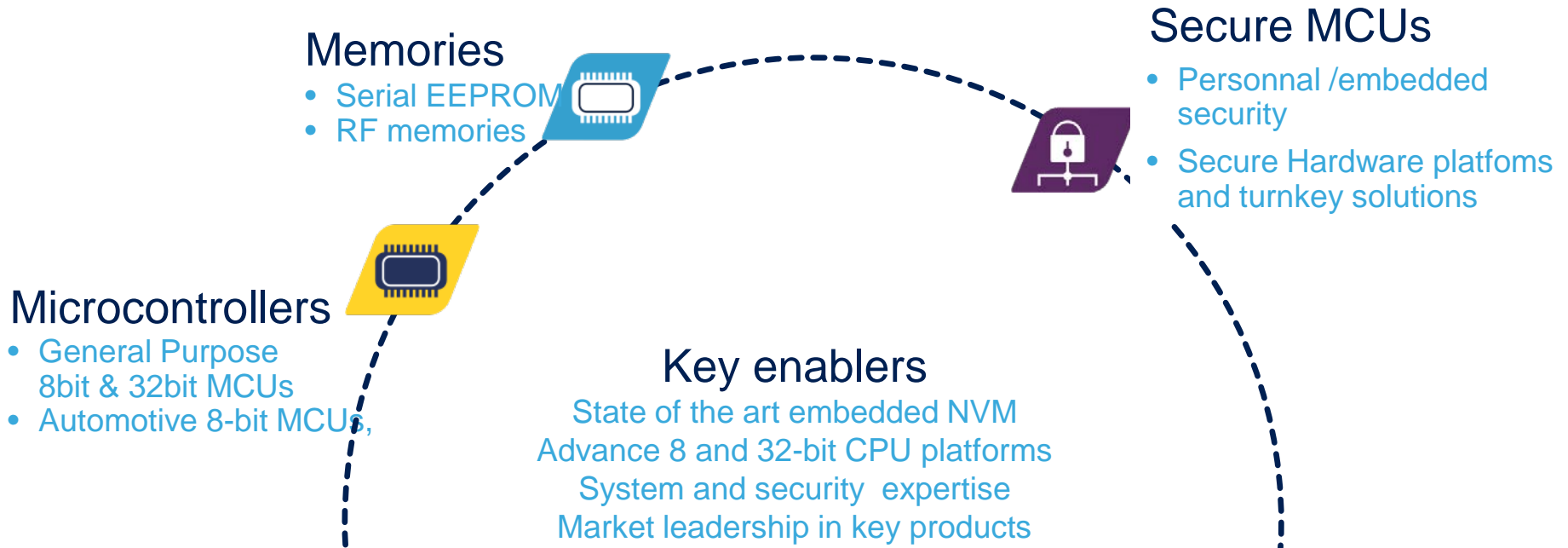


MDG-MMS group

Stage proposals on STM32 microcontrollers

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Automotive



Healthcare



Industrial/Smartgrid



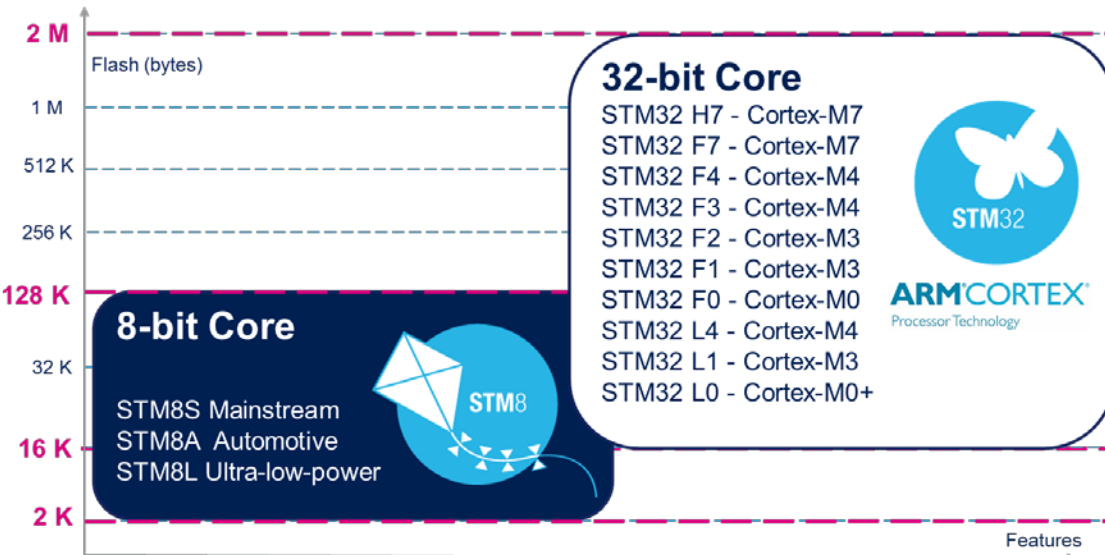
Security



Consumer

General Purpose MCUs

A Wide range of Product sales Types embedding a rich set of Digital & Analog Peripherals
Enabling selection flexibility on Embedded Flash size as well as performances



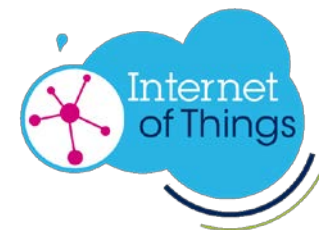
<p>Real-time performance</p> <p>STM32 Dynamic Efficiency™, ART Accelerator™, Chrom-ART Accelerator™, CCM-SRAM, L1-Cache Multi-AHB bus matrix, Excellent real-time Zero-wait state execution performance from Flash</p>	<p>Outstanding power efficiency</p> <p>Dynamic Power 40 – 150 uA/Mhz Stop down to < 1 uA Stand By down to < 300 nA Shutdown down to < 20 nA</p>	<p>Reach Set of peripherals</p> <p>USB-OTG High speed, Ethernet, CAN, DFSDM, HR timer, LCD-TFT controller, SRAM interface, crypto/hash processor, true RNG*, PGA, 16-bit ΣΔ ADC and 12-bit ADC (up to 5 MSPS), external memory interface, CEC, SAI</p>	<p>Maximum integration</p> <p>Reset circuitry, voltage regulator, internal RC oscillator, PLL, WLCSP packages</p>
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Smart Industry

Smart Home

Smart City

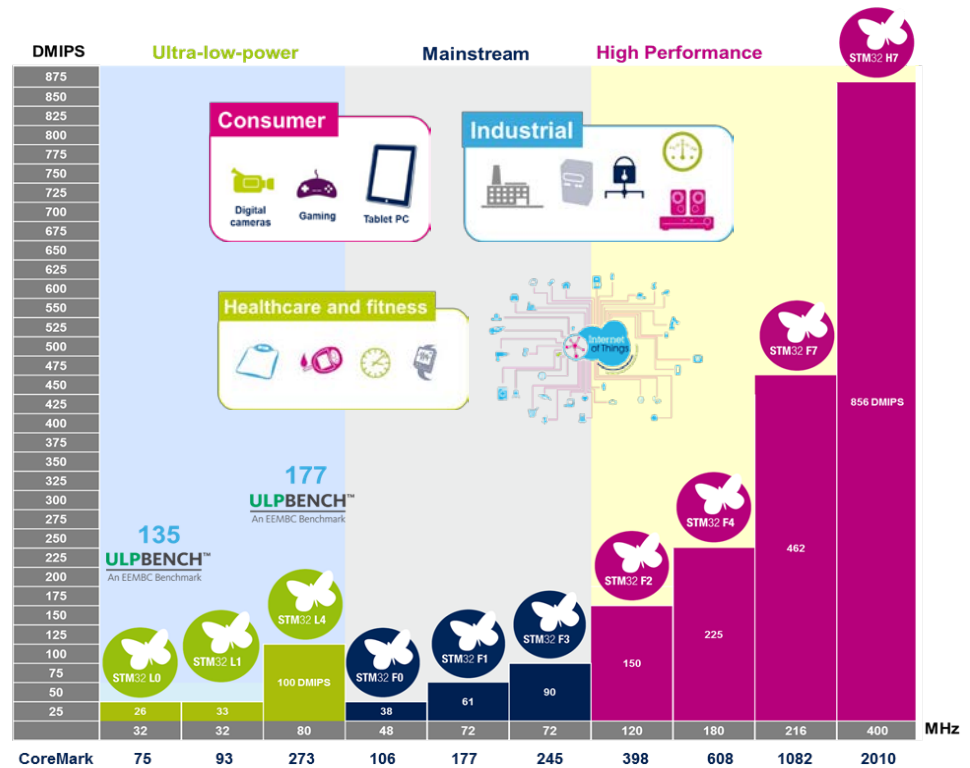
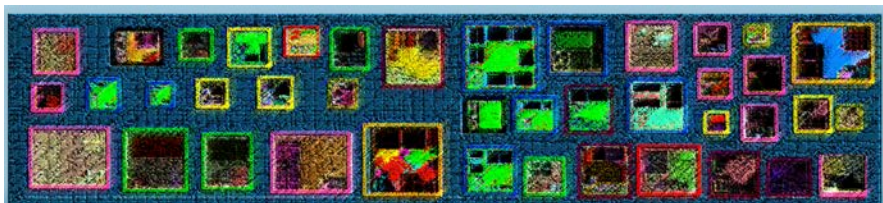
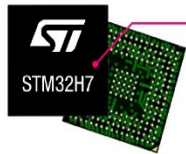
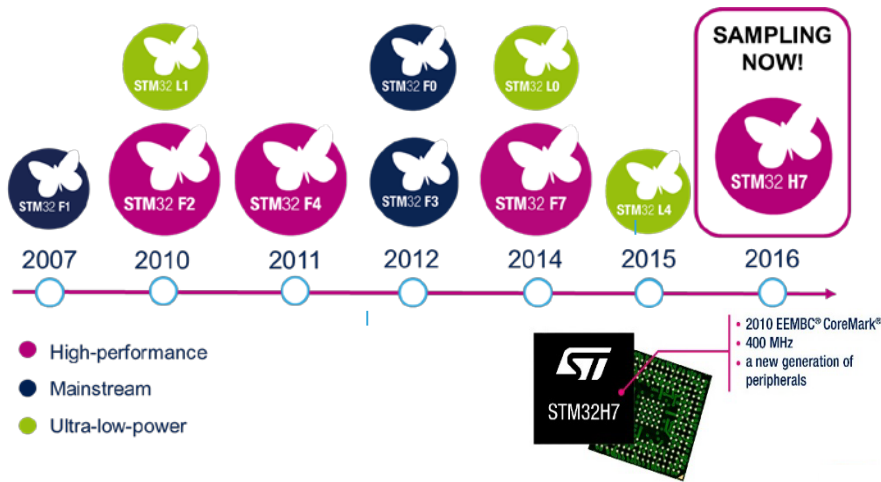
Smart Things



Over 4 Billion Devices Delivered to Broad Range of Markets

STM32 ARM Cortex-M Based MCUs

Keep Innovating! : Highest CoreMark Result on ARM Cortex-M



STM32 MCU Design Challenges

5

PRIORITIES

High Performance

Performance: > 800 DMIPS
Dynamic Power efficiency
Static Power efficiency
Die size

Ultra Low Power

Dynamic Power efficiency
Static Power efficiency
Performance: > 100 DMIPS
Die size

Main Stream

Dynamic Power Efficiency
Ratio Performance/Power
Die Size
Static Power Efficiency

CHALLENGES

1. Power, Robustness, Size Co-Optimization

- Multi-VT / Multi-site / Multi-voltage / Multi Process scenarios
- Ultra low power clock tree
- EMC , Robustness, Safety Compliance

2. Multi-Voltage Design Complexity

- Fragmented voltage area hierarchically/topologically
- Voltage scaling
- Always On Cells (isolated / not isolated)

3. System Performances & ARM Cortex-M Cores integration Objectives

- Realizing maximum system performance
- Achieving ultra-low power

Broad diversity of challenges, very aggressive time schedules